describe

ATD5833It is an intelligent stepper motor driver with a built-in decoder. Its output driving capability reaches30V ±2.5A, the highest support16Subdivision, and interpolation subdivision can be realized at the same time.

The decoder isATD5833Ease of use is key.STEPA simple input pulse from the pin can make the motor complete one step, eliminating the need for a phase sequence table, high-frequency control lines, and complex programming interfaces. This makes it more suitable for applications where complex microprocessors are unavailable or overloaded.

ATD5833Support voltage attenuation mode, with256Automatic interpolation and subdivision make the motor completely silent, achieving smooth motion even at full-step operation. It also supports mixed current decay to provide high torque output.

ATD5833Supports automatic half-flow locking function.STEPWhen the voltage changes, the output current is automatically halved to reduce the system lock power consumption.

Synchronous rectification control circuit improvesPWMThe internal protection circuit includes over-temperature protection, under-voltage lockout protection and over-current protection.

ATD5833Currently available with thermal padsQFN28The package can effectively improve the heat dissipation performance, and it is a lead-free product that meets environmental protection standards.

Model selection

Order Model	Encapsulation	Packaging Information
ATD5833QNN	QFN5*5-28	Taping,5000Pieces/Plate

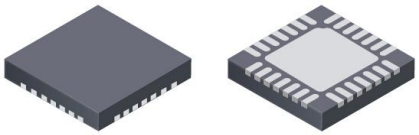
Features

- Two-phase four-wire bipolar stepper motor driver
- Low on-resistance$R_{DS(ON)}$,2.5APeak current output
- SimpleSTEP/DIRInterface, maximum support16Segmentation
- OptionalUARTinterface
- Support interpolation and subdivision function, automatically interpolate to256Segmentation
- Support voltage attenuation, ultra-quiet operation, smoother movement
- Supports mixed current decay and high torque output
- Support half-flow locking function
- Support low power standby function
- Compatible3.3Vand5VLogic Level
- Complete protection functions

application

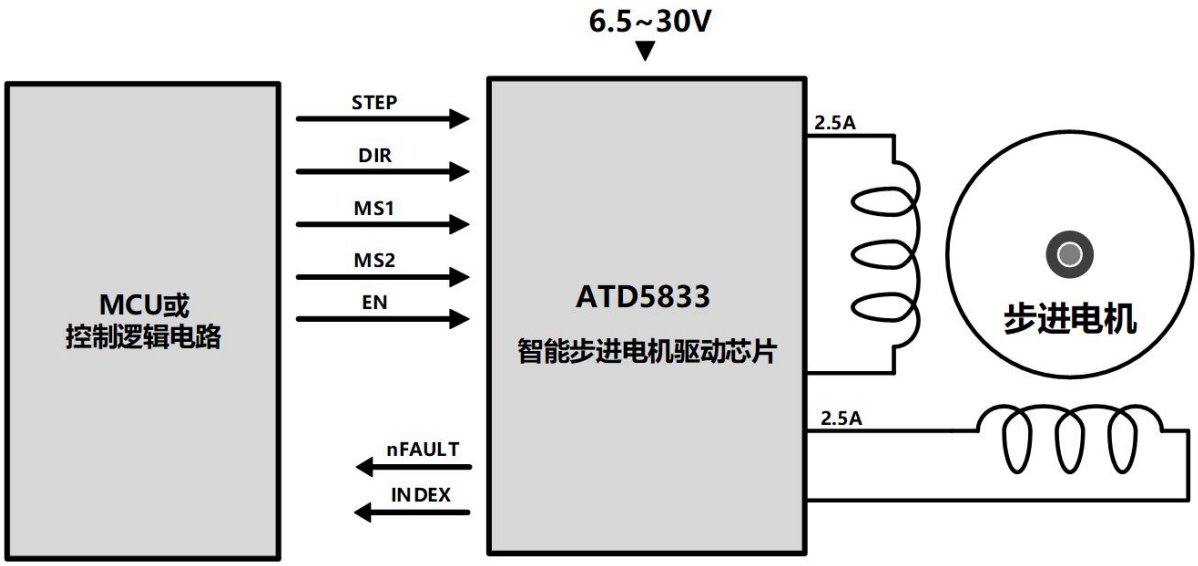
- Printers, scanners and other automated office equipment
- 3Dprinter
- Game consoles, robots, medical equipment
- Security,ATM

Package



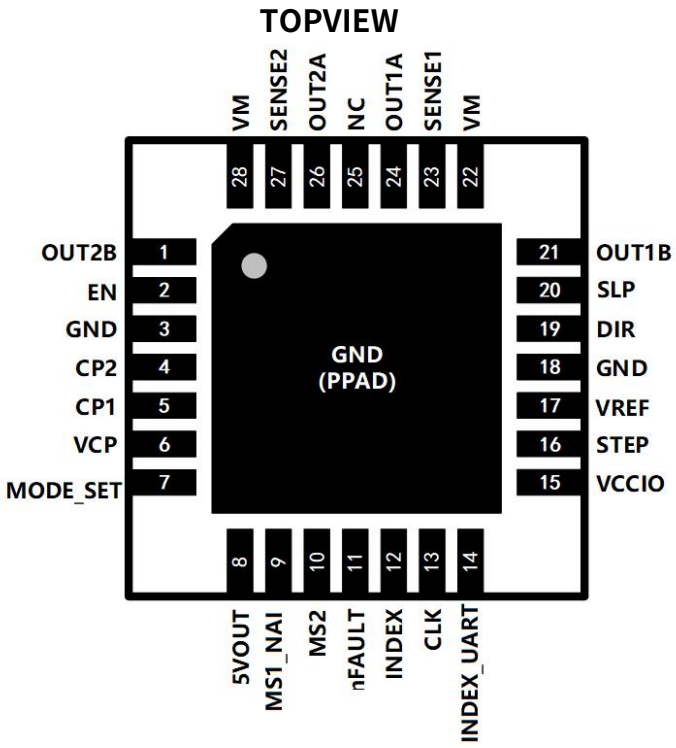
QFN28

Typical application schematic diagram



date	Version	content
2020.05	V1.0	Initial version

Pin Definition

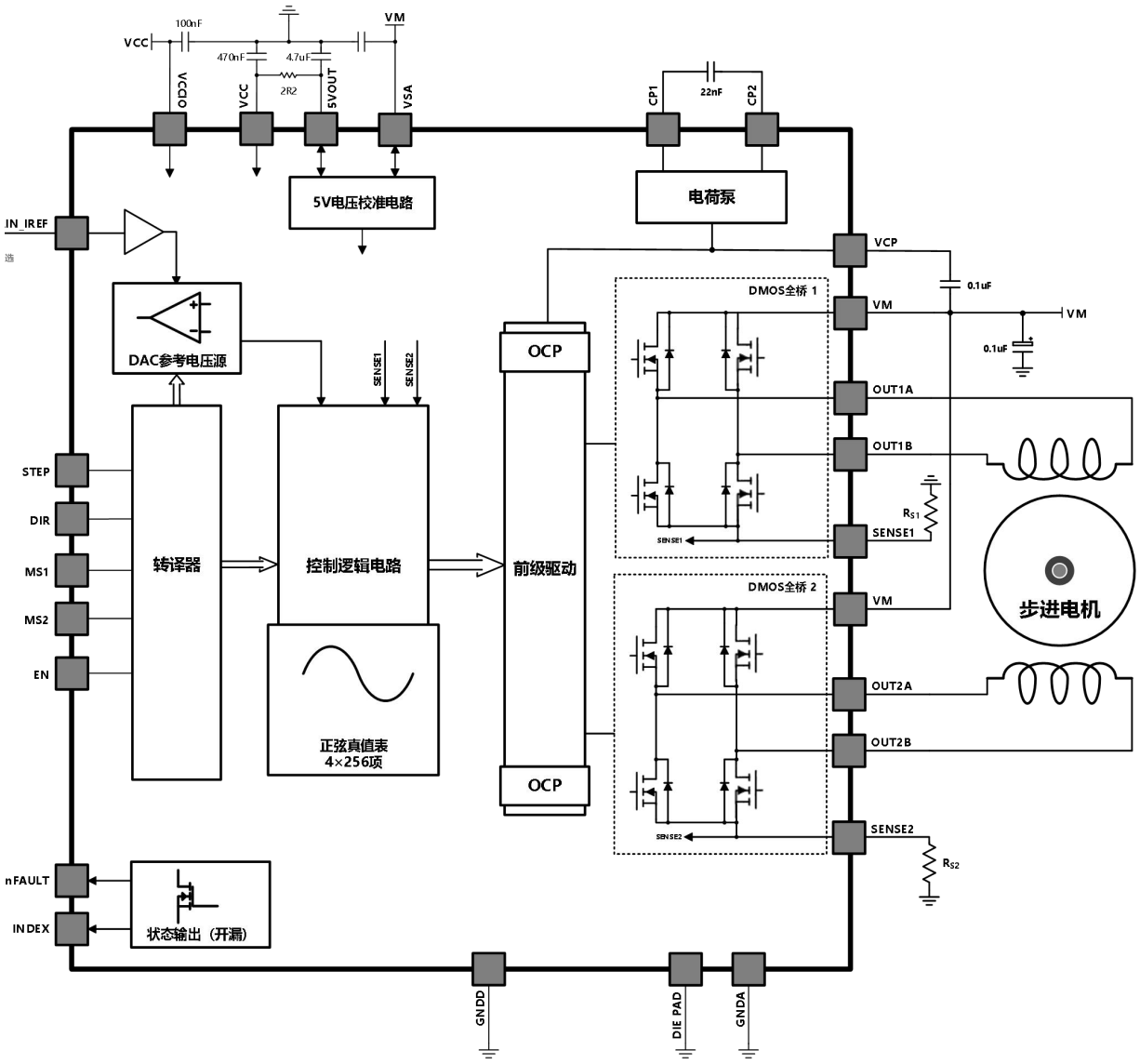


Pin List

Pin Name	Pin number	Pin Description
OUT2B	1	Full Bridge2OutputBend
EN	2	Enable input, low active
GND	3,18	land(GNDThe pins must be connected to the back of the device throughPADGrounds are connected together externally)
CP2	4	Charge pump flying capacitor terminal2
CP1	5	Charge pump flying capacitor terminal1
VCP	6	Charge pump energy storage end
MODE_SET	7	Mode selection, internal pull-down, floating or ground selectionSTEP/DIRInterface, high level selectionUARTinterface
5VOUT	8	internal5VRectified output, need to be connected2.2uFCapacitor filtering
MS1_NAI	9	Segment selection input1,UARTThe address input of the interface,STEP/DIRIt is recommended to leave the interface input floating
MS2	10	Segment selection input2,STEP/DIRIt is recommended to leave the interface input floating
nFAULT	11	Fault detection indication output
NAO	12	UARTNext address output of the interface
CLK	13	CLKInput, if using internal clock, please ground
INDEX_UART	14	Step index indication output,UARTData input of the interface
VCCIO	15	Digital power supply, connected3.3Vor5Vpower supply
STEP	16	STEPPulse input
VREF	17	Analog reference voltage input
DIR	19	Direction control signal input
SLP	20	Low power standby input, internal pull-down, high level valid
OUT1B	twenty one	Full Bridge1OutputBend
VM	22,28	Power supply (power filtering is required)

SENSE1	twenty three	Full Bridge1Current sensing resistor terminal
OUT1A	twenty four	Full Bridge1OutputAend
OUT2A	26	Full Bridge2OutputAend
SENSE2	27	Full Bridge2Current sensing resistor terminal
PAD	-	The bottom exposed pad is connected to the system ground for heat dissipation

Functional module block diagram



Circuit operating limitsat T_A= 25°C

parameter	symbol	Test conditions	scope	unit
Maximum supply voltage	V_S		35	V
Output current	I_{OUT}		±2.5	A
Logic input voltage	V_{IN}		- 0.3 to 5.5	V
Logic supply voltage	VCC_IO		- 0.3 to 5.5	V
Motor output voltage	V_{OUT}		- 2.0 to 35	V
Current sense voltage	V_{SENSE}		- 0.5 to 0.5	V
Reference voltage	V_{REF}		2.5	V
Working temperature	T_A	Range S	- 40 to 85	°C
Maximum junction temperature	T_J(max)		150	°C
Storage temperature	T_{stg}		- 55 to 150	°C

Thermal resistance characteristicsat T_A= 25°C

Heat metering	QFN	unit
	28PINS	
θ_{JA} -Thermal resistance from silicon core to ambient(*)	41	°C/W

(*)The thermal resistance from the silicon core to the environment under natural convection conditions is calculated byJESD51-7Specified inJEDECHigh standardsKThe simulation is carried out on the circuit board, and the environmental conditions are as follows

JESD51-2aAs described in.

Recommended operating conditionsat T_A= 25°C

parameter	symbol	Minimum	typical	maximum	unit
Load supply voltage	V_S	6.5	-	30	V
Logic supply voltage	VCC_IO	3	-	5. 5	V
Output current setting	I_{OUT}	0	-	2.0	A

Recommended peripheral settings

1、CPcapacitance:0.1uF/50V **2**、

VCPcapacitance:0.1uF/50V

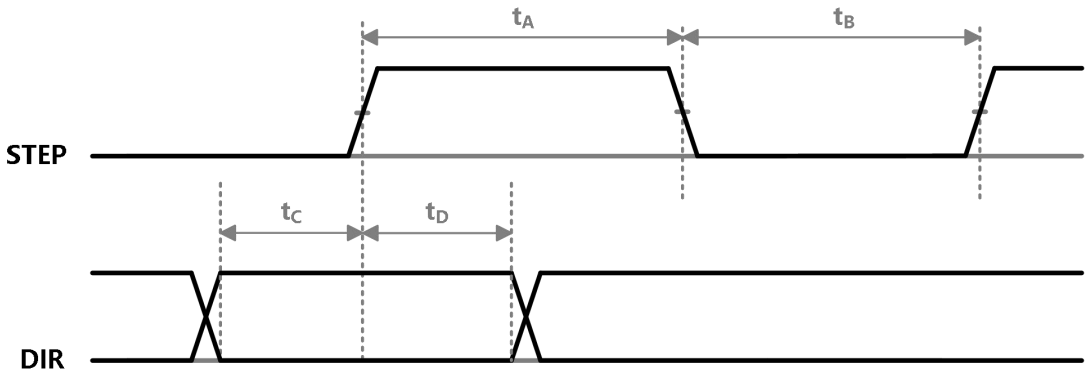
3、5VOUTFilter capacitor:4.7uF/16V

4、VCCFilter capacitor:470nF/16V, concatenate2.2RResistor connection5VOUT

Electrical characteristicsat T_A= 25°C, V_S= 24V

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
Output Driver						
Load power supply range	V_S	Working status	6.5	-	30	V
Logic power supply range	V_{CC_IO}	Working status	3.0	-	5.5	V
Load power supply static power consumption	I_{VS}	f_{PWM}<50kHz	-	15	twenty two	mA
Logic power supply static power consumption	I_{VCC_IO}	f_{PWM}<50kHz	-	-	8	mA
5VRectified output	5VOUT		4.8	5	5.2	V
Logic Input						
Logic input level	$V_{IN(1)}$		V_{IO}*0.7	-	-	V
	$V_{IN(0)}$		-	-	V_{IO}*0.3	V
Logic input hysteresis	$V_{HYS(IN)}$	VCC_IOPercentage	5	12	19	%
Internal pull-up and pull-down resistors (xThree-state input)	R_{PU}、R_{PD}		133	166	200	k-
Reference voltage input range	V_{REF}		0	-	2.5	V
BRxCurrent sensing peak voltage	VSRT		-	0.32	-	V
HBridge output						
Output on-resistance	$R_{DS(ON)}$	High side,I_{OUT}=-1A	-	170	240	m-
		Low side,I_{OUT}=1A	-	170	240	m-
Body diode forward voltage drop	V_F	High side,I_F=-1A	-	-	1.2	V
		Low side,I_F=1A	-	-	1.2	V
Dead time	t_{DT}		160	220	280	ns
Output upper tube turn-on rise time	tr	Output pull-down12Ω	-	230	-	ns
Output lower tube turn-on fall time	t_f	Output pull-up12Ω	-	150	-	ns
Protection function						
Overcurrent protection	I_{OCPST}		3	-	-	A
Overtemperature shutdown	T_{TSD}		-	150	-	°C
Overtemperature hysteresis	T_{TSDHYS}		-	35	-	°C

Requirements on circuit control signal timing:(TA= +25°C, VCCIO = 3.3 V,The logic level isVCCIOorGND)



Control signal timing diagram

Duration	symbol	Typical values	unit
Minimum high level pulse width of step pulse	t_A	1	us
Minimum high level pulse width of step pulse	t_B	1	us
Setup time	t_C	200	ns
Keep time	t_D	200	ns

Input pin configuration

MS1、MS2: Subdivision and attenuation method selection

MS2	MS1	Segmentation	Automatic interpolation	Attenuation method
GND	GND	1	N	Mixed current decay
GND	VCCIO	2	N	
GND	Dangling	2	Y,arrive256Segmentation	
VCCIO	GND	4	N	
VCCIO	VCCIO	16	N	
VCCIO	Dangling	4	Y,arrive256Segmentation	
Dangling	GND	16	Y,arrive256Segmentation	
Dangling	VCCIO	4	Y,arrive256Segmentation	Voltage decay
Dangling	Dangling	16	Y,arrive256Segmentation	

EN: Enable configuration

EN	Output Enable Description
GND	Output Enable
VCCIO	Output off
Dangling	Output enable, and half-current lock function is enabled at the same time

Module Function Description

Device Operation

ATD5833It is a micro stepper motor driver with an integrated decoder that is easy to use and requires only a small number of control lines. Its design allows bipolar stepper motors to operate in full, half,1/4and1/16Step work. EachHThe bridge has a fixed decay timePWMCurrent control circuit to limit its NChannelDMOSThe load current of the power tube is at a designed value. The full-bridge output current of each step is determined by the external current-sense resistor (R_{S1}andR_{S2}) value, reference voltage (V_{REF})andDAC(The output voltage of the decoder is controlled in turn.

At power-up or reset, the decoder willDACThe polarity of the phase current is set to the initial zero state, and the current regulators of both phases work in mixed decay mode.STEPport, the decoder automaticallyDACSequence to the next level and current polarity. (The microstepping phase sequence table gives the current step sequence).

When stepping, ifDACThe output level of the currentHThe full bridge enters mixed decay mode. If DACIf the output level is higher than or equal to the previous level, the currentH The full-bridge enters slow decay mode. Automatic current decay selection improves microstepping performance by reducing current waveform distortion caused by the motor's back EMF.

Microstepping selection (MS1、MS2)

The microstepping accuracy is determined byMS1、MS2The logic input voltage is determined as listed in the input pin configuration.MSxWhen changing the step mode, until the nextSTEPIt only works on the rising edge of .

If the step mode is changed and the decoder is not reset, it will The position must be maintained. To prevent lost steps, it is important to select a step position that applies to all step modes before changing step modes. When the device loses power or restarts due to overtemperature or overcurrent, the decoder is placed at the zero position, which is the default common position for all step modes.

Mixed decay operation

When the system is operating normally after power-on reset,MSxConfiguration and step sequence,HThe bridge operates in mixed decay mode. During mixed decay, when a predetermined value is reached,ATD5833Initially enters fast decay mode, fast decay time accounts for fixed decay timet_{OFF}of31.25%, and then turns to slow decay until the fixed decay time ends.

Generally, mixed attenuation is just a process of reducing the current in the winding from a high

For most loads, the automatic selection of the mixed decay mode is convenient because it can reduce the ripple when the current rises and prevent the ripple when the current falls. The lost step.

Especially in some very low speed micro-stepping applications, it is very necessary If the back EMF in the winding is insufficient, the current in the load will increase rapidly, resulting in lost steps. Even if lost steps are not a problem, it is recommended to use the automatic selection of mixed decay mode because it reduces current ripple. Please refer to the Fixed Decay Time section for a detailed description.

Low current microstepping

In some applications, the on-time is too short to allow the output current to flow freely.

To prevent this from happening, the device can operate in mixed decay mode in both the rising and falling directions of the current waveform.

STEPenter

STEPThe rising edge of the signal triggers the valid signal, which is controlled by the translator.STEPThe rising edge trigger causes the motor to change in one step. DACThe input and the direction of the current flowing through the coil; the current magnitude and rotation angle of each step are determined byMS1、MS2Input logic level control.

Direction Control (DIR)

DIRInput controls the direction of rotation of the motor.STEPBefore the rising edge of the signal triggers, anyDIRThe changes above will not affect the circuit.

internalPWMCurrent control

Every oneHThe bridge has a fixed decay timePWMThe current control circuit limits the load current to a designed value.I_{TRIP}If an external current sense resistor is used, initially, the pair of diagonal resistorsDMOS (a pair of upper and lower bridge arms) are in output state, and current flows through the motor winding andSENSExThe current sampling resistor connected to the pin,R_{Sx}When the voltage on the sampling resistor is equal toDACWhen the output voltage of the current sampling comparator is PWMThe latch is locked, thereby turning off the source driver (upper bridge arm) and entering slow decay mode; or turning off the source driver and the sink driver (upper and lower bridge arms) at the same time to enter fast or mixed decay mode, causing a circulating current or current to flow back to the source end. This circulating current or return current will continue to decay until the fixed decay time ends. Then, the correct output bridge arm is started again, the motor winding current increases again, and the entirePWMThe cycle is completed. Among them, the maximum current limit is determined by the sampling resistor$R_{Sx}$and the input of the current sampling comparator.V_{REF}controlled$I_{TripMAX}$(A)Determined by the following formula:

$$I_{TRIP}\text{max} = V_{REF} / (8 \times R_S)$$

The actual current in each step is a percentage of the maximum current, which is approximately:

$$I_{TRIP} = \%_0 I_{TRIP}max$$

(The microstepping phase sequence table gives the maximum current percentage for each step)

Notice:SENSExThe maximum voltage on the pin cannot exceed0.5V.

Charge Pump (CP1andCP2)

The charge pump is used to generate aVMvoltage to drive sourceDMOSThe gate. A0.1uFThe ceramic capacitor is connected toCP1、 CP2 Between, the purpose of the charge pump is achieved.0.1uFCeramic capacitors connected toVCP、VMBetween, used to store charge to drive the source DMOSdevice.

The capacitance value needs to beClass2medium,±15% Maximum fluctuation or withstand voltageRLevel, according toEIA.

Enable Input (EN):

This input controls allFETWhen it is logic high, the output is off. When it is logic low, the internal Control enable is effective. Decoder inputSTEP,DIR,MS1、 MS2 and internal timing logic, all valid and independent ofENenter.

SHUTDOWNShutdown

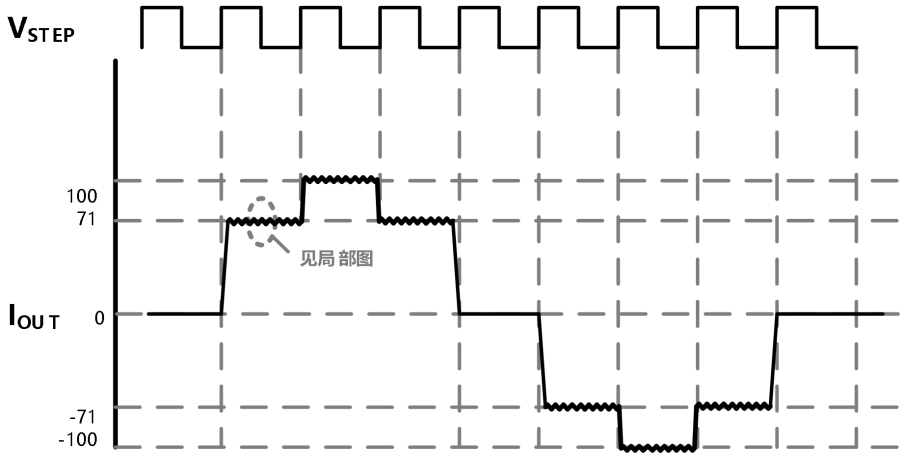
When the circuit is over-temperature protected orVCPThe undervoltage lockoutSHUTDOWNThe function is working normally, the normal function of the circuit is disabled until the circuit is disconnectedSHUTDOWNcondition.

Synchronous Rectification

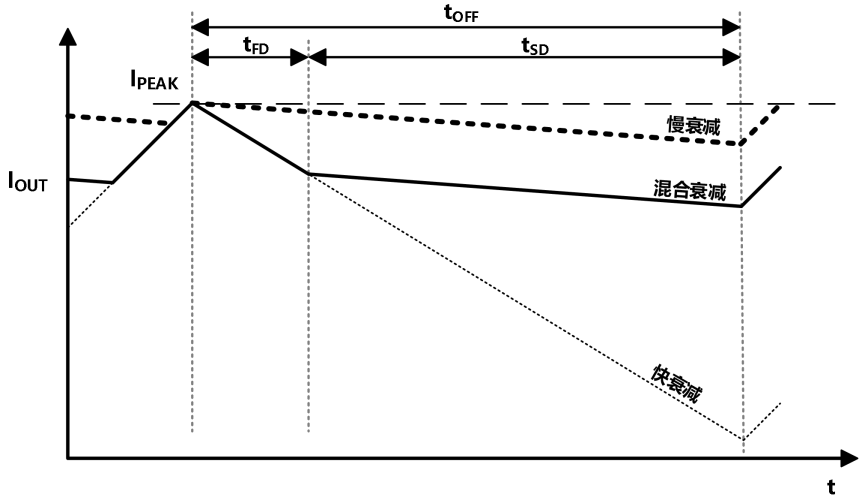
During the current decay period, the synchronous rectification function turns on the correspondingFET becauseFETThe on-resistance is low, effectively short-circuiting the body diode. This effectively reduces power consumption and, in many applications, eliminates the need for an external Schottky diode.0When , the synchronous rectification is turned off, thus preventing the load current from reversing.

INDEXOutput

INDEXThe output outputs a pulse after the motor has run one full step, that is, one pulse every four full steps. It indicates the internal sequencer microstep0The position of the power-on position. Combining it with a mechanical zero switch can achieve a more accurate zero return.



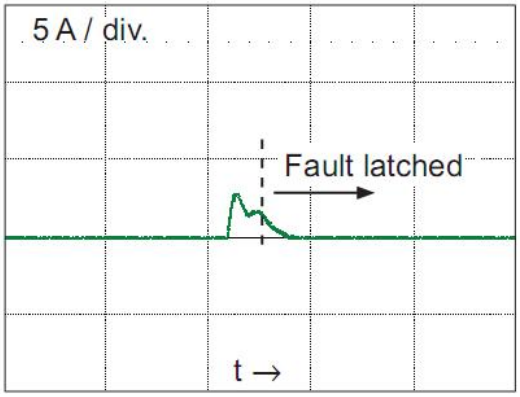
Current step example diagram



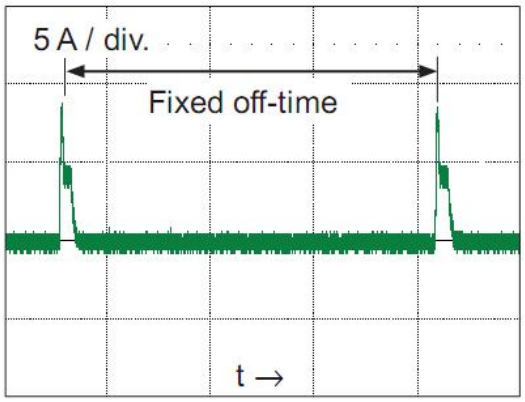
Decay current local diagram

symbol	nature
t_{off}	Device fixed off time
I_{PEAK}	Maximum output current
t_{SD}	Slow decay interval
t_{FD}	Fast decay range
I_{OUT}	Device output current

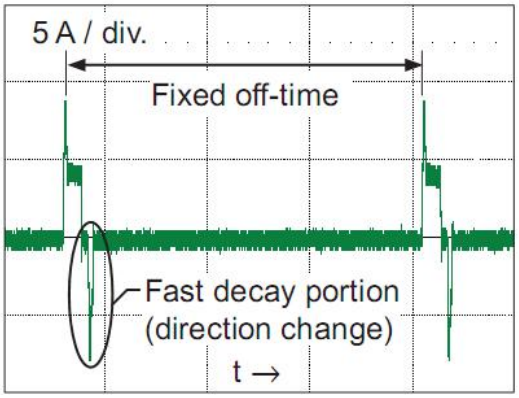
Protection circuit



Short circuit to ground



Output short circuit in slow decay state

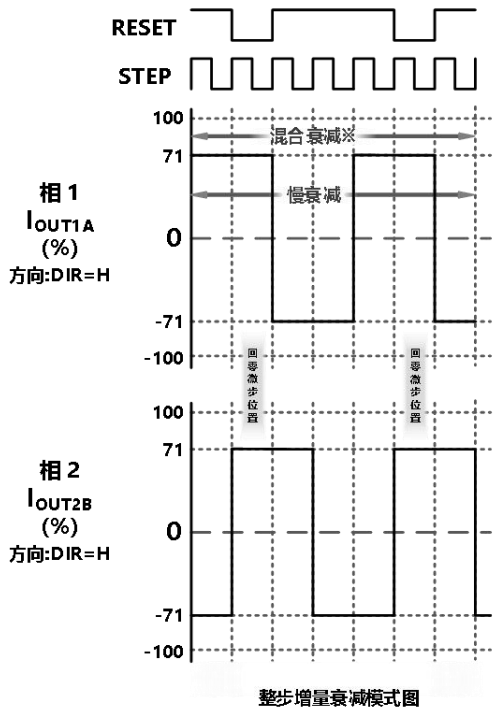


Output short circuit in mixed decay state

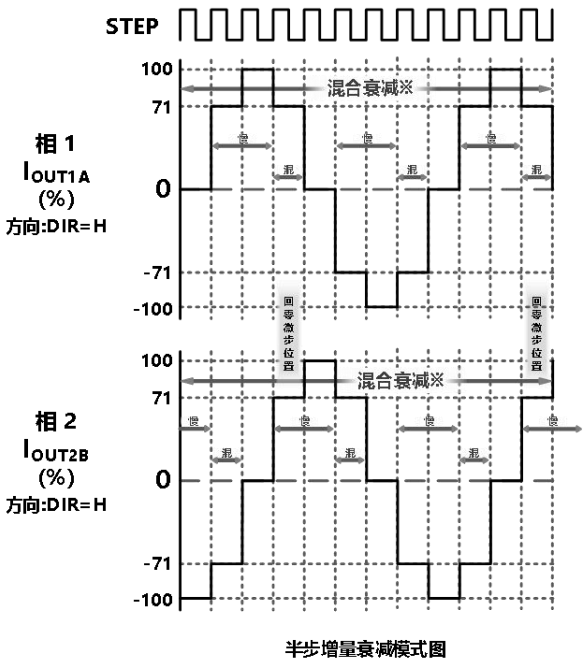
Output short circuit and short circuit to ground protection

If the two motor output pins are shorted or any output pin is shorted to ground, the driver will detect the overcurrent event and then shut down the output to prevent the device from burning out. When a short circuit to ground occurs, the driver will remain in the off state untilnSLEEPEnter high level.

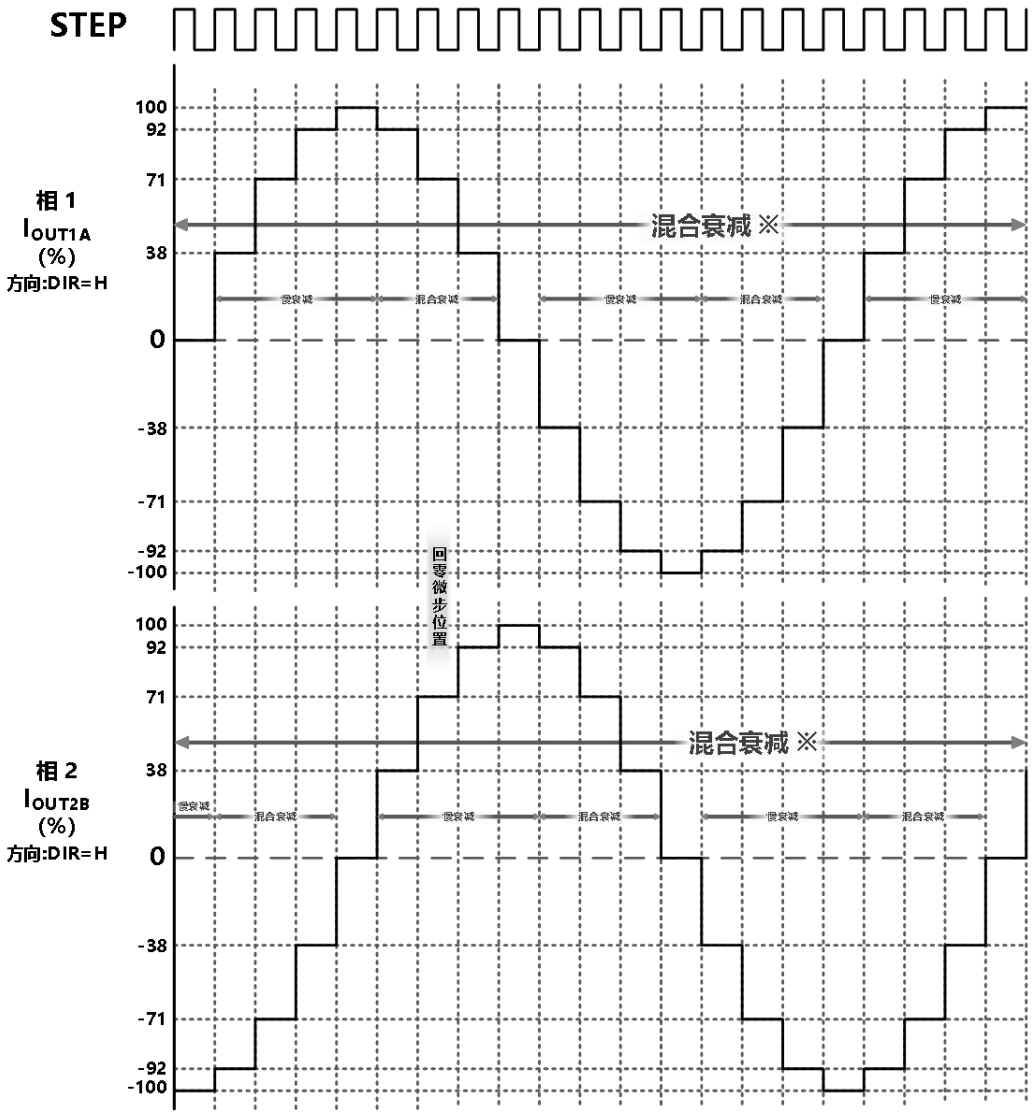
When the two outputs are shorted together, the current flows through the sense resistor. After a blanking time, the voltage across the sense resistor exceeds the maximum voltage due to overcurrent. This causes the driver to enter fixed decay mode. After a fixed decay time, the device resumes protection. In this case, the device is fully protected from overcurrent, but short circuits can recur based on the fixed decay period. When a load short occurs, the mixed decay effect causes a forward or reverse current spike to be observed during current switching. In both cases, the overcurrent protection circuit protects the driver from burnout.



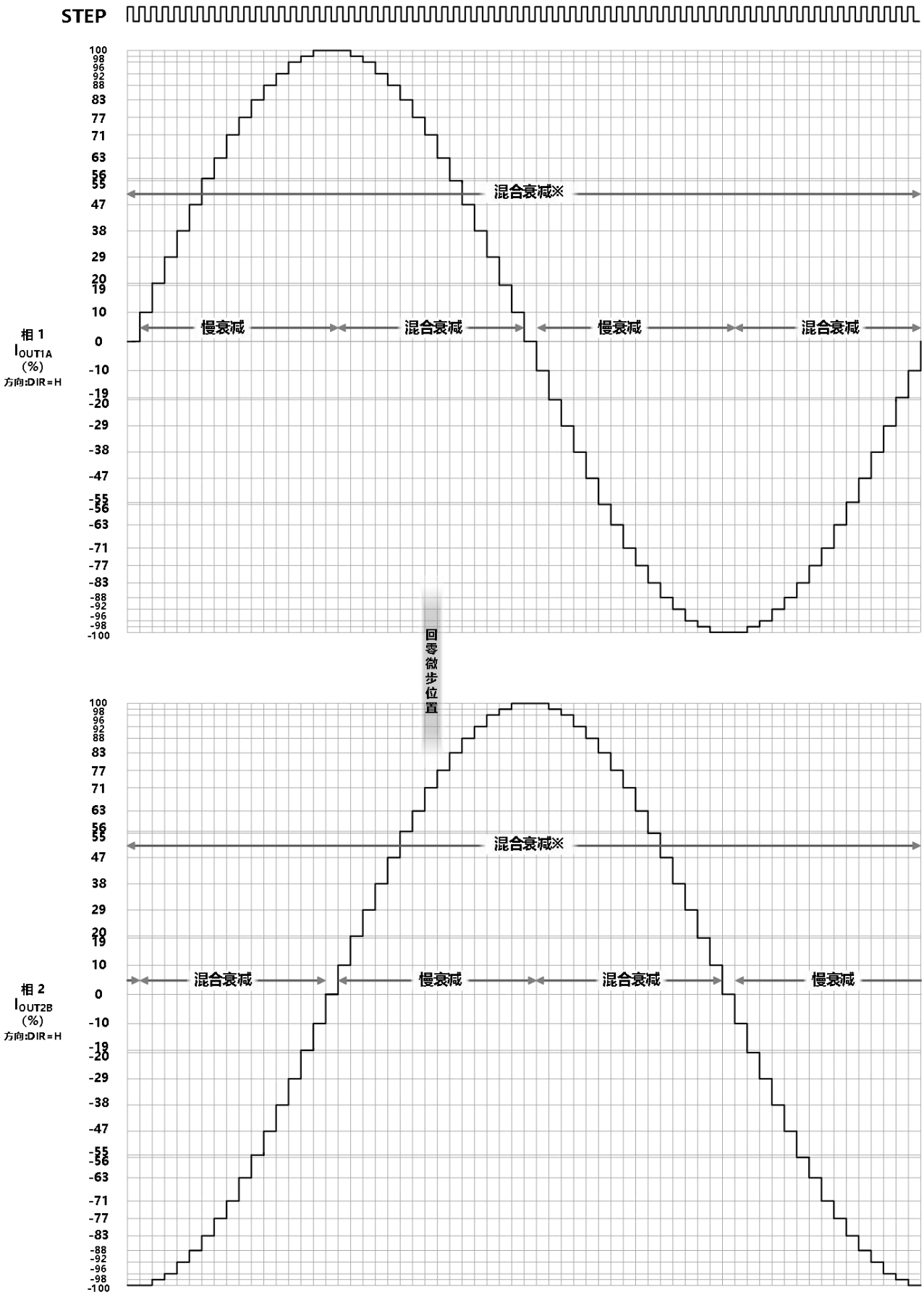
整步增量衰减模式图



半步增量衰减模式图



四分之一步增量衰减模式图



十六分之一步增量衰减模式

Microstepping phase sequence table

Return to zero microstep position at step angle45°Department;DIR = H

1/16step	1/4step	Half Step	Whole step	Step Angle(°)	1Phase current (%)	2Phase current (%)
1	1	1		0.00	100	0
2				5.6	100	10
3				11.3	98	20
4				16.9	96	29
5	2			22.5	92	38
6				28.1	88	47
7				33.8	83	56
8				39.4	77	63
9	3	2	1	45	71	71
10				50.6	63	77
11				56.3	55	83
12				61.9	47	88
13	4			67.5	38	92
14				73.1	29	96
15				78.8	19	98
16				84.4	10	100
17	5	3		90	0	100
18				95.6	- 10	100
19				101.3	- 20	98
20				106.9	- 29	96
twenty one	6			112.5	- 38	92
twenty two				118.1	- 47	88
twenty three				123.8	- 56	83
twenty four				129.4	- 63	77
25	7	4	2	135	- 71	71
26				140.6	- 77	63
27				146.3	- 83	55
28				151.9	- 88	47
29	8			157.5	- 92	38
30				163.1	- 96	29
31				168.8	- 98	19
32				174.4	- 100	10
33	9	5		180	- 100	0

34				185.6	- 100	- 10
35				191.3	- 98	- 20
36				196.9	- 96	- 29
37	10			202.5	- 92	- 38
38				208.1	- 88	- 47
39				213.8	- 83	- 56
40				219.4	- 77	- 63
41	11	6	3	225	- 71	- 71
42				230.6	- 63	- 77
43				236.3	- 55	- 83
44				241.9	- 47	- 88
45	12			247.5	- 38	- 92
46				253.1	- 29	- 96
47				258.8	- 19	- 98
48				264.4	- 10	- 100
49	13	7		270	0	- 100
50				275.6	10	- 100
51				281.3	20	- 98
52				286.9	29	- 96
53	14			292.5	38	- 92
54				298.1	47	- 88
55				303.8	56	- 83
56				309.4	63	- 77
57	15	8	4	315	71	- 71
58				320.6	77	- 63
59				326.3	83	- 55
60				331.9	88	- 47
61	16			337.5	92	- 38
62				343.1	96	- 29
63				348.8	98	- 19
64				354.4	100	- 10

Layout Considerations

PCBThe board should be covered with a large heat sink, and the ground connection should have a wide ground trace. To optimize the circuit's electrical and thermal performance, the chip should be directly attached to the heat sink.

Power supply for motorVM, should be connected to no less than47uFThe electrolytic capacitor is coupled to the ground, and the capacitor should be placed as close to the device as possible.dv/dtTo prevent capacitive coupling caused by the conversion, the output wiring of the driver circuit should be kept away from the wiring of the logic control input terminal. The wiring of the logic control terminal should use low-impedance routing to reduce noise caused by thermal resistance.

Ground wire setting

AGNDandPGNDThe ground traces must be shorted outside the chip. All ground traces should be connected together and kept as short as possible. A star-shaped, diverging ground trace layout beneath the device is an optimal design.

Adding a copper heat sink under the ground line will further optimize circuit performance.

Current sampling settings

In order to reduce the error caused by parasitic resistance on the ground line, the motor current sampling resistorR_SThe ground wire should be set up separately to reduce the error caused by other factors. The separate ground wire should be connected to the star-shaped ground bus. The connection should be as short as possible.R_S,becauseR_S Pressure drop on$V\text{-}I\text{-}R_S$Less than0.5V,PCBThe connection voltage drop on0.5VThe voltage will become non-negligible and this needs to be taken into account.

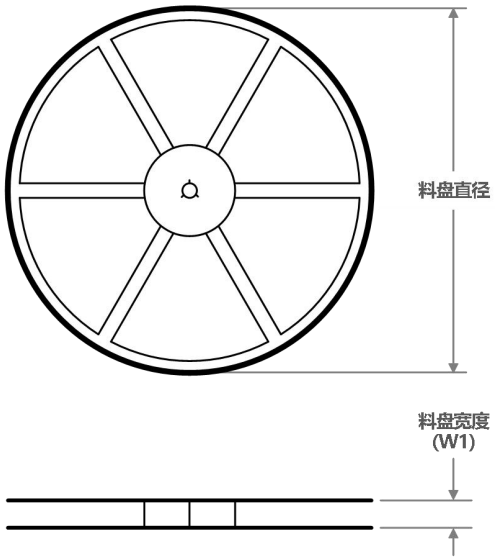
PCBTry to avoid using test adapter sockets, as the connection resistance of the test socket may changeR_SThe size of the circuit will cause errors.R_SThe value is chosen according to the following formula:

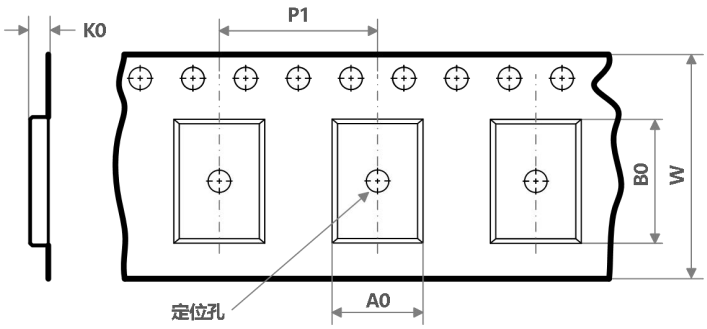
$$R_S\text{-}0.5/I_{TRIP}\text{max}$$

Thermal protection

When the internal circuit junction temperature exceeds150°CWhen the over-temperature protection circuit starts to work, it shuts down the internal drive circuit. The over-temperature protection circuit only protects against problems caused by excessive circuit temperature, and does not affect the output short circuit. The threshold window size of thermal shutdown is35°C.

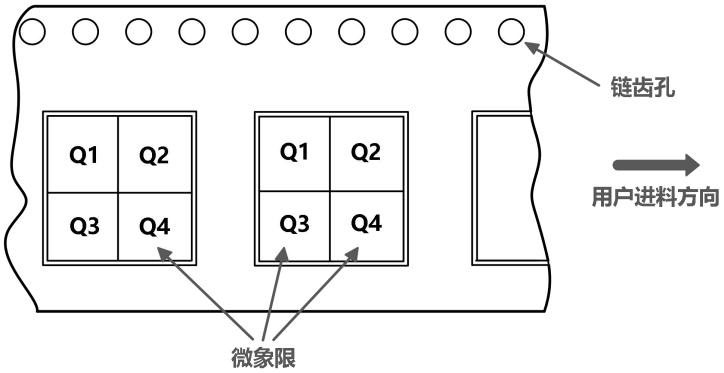
Taping reel information





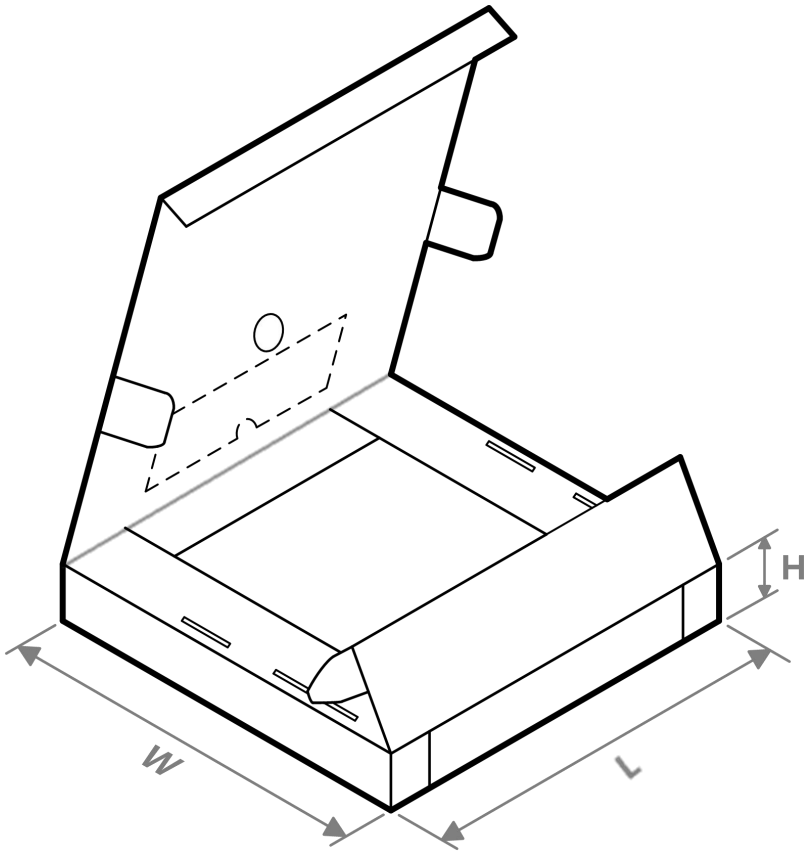
A0	Trough width
B0	Trough length
K0	Trough thickness
W	Overall width of carrier tape
P1	Center distance between adjacent slots

Tape PIN1 Azimuth Quadrant Assignment



Device	Encapsulation type	Encapsulation Logo	Pins number	SPQ	Feed tray diameter (mm)	Feed tray width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 quadrant
ATD5833QNN	QFN	QNN	28	5000	330	12	6	5.7	1.5	8	12	Q2

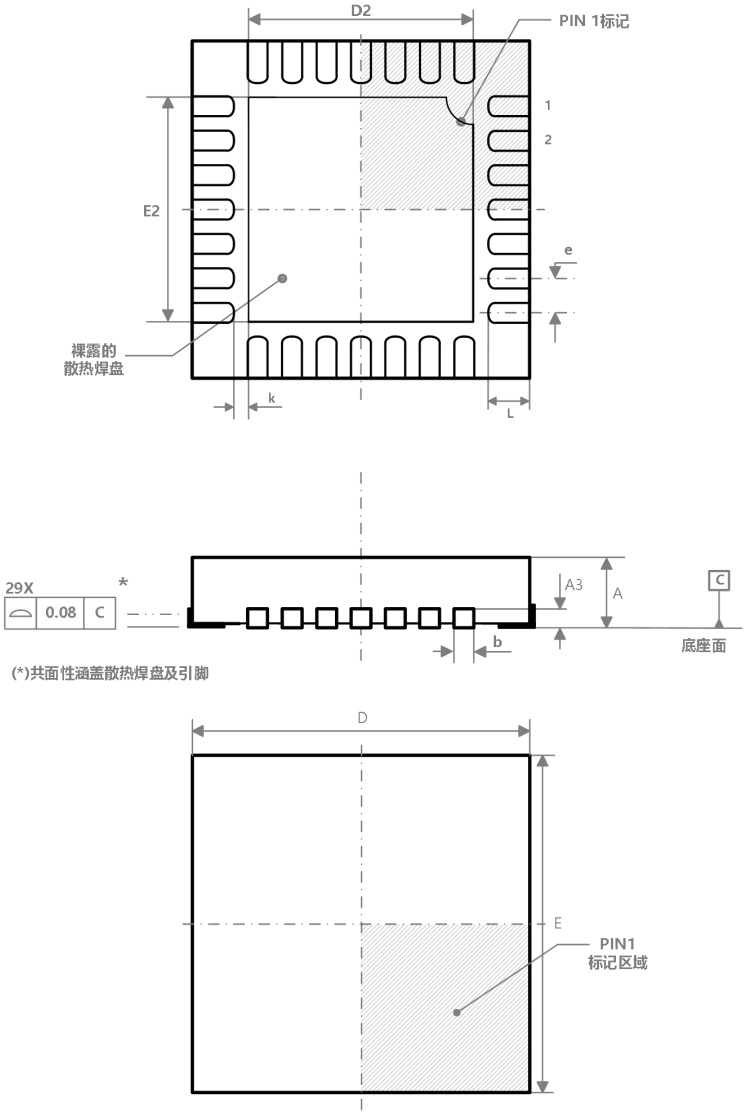
Tape reel packaging size



Device	Package Type	Package marking	Number of pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ATD5833QNN	QFN	QNN	28	5000	365	365	70

Package information

QFN28



parameter	millimeters (mm)		
	MIN	NOM	MAX
E	4.9	5.00	5.10
D	4.9	5.00	5.10
E2	3.00	3.15	3.25
D2	3.00	3.15	3.25
b	0.18	0.25	0.30
e	0.50 BSC		
k	0.2	-	-
A	0.70	0.75	0.80
A3	0.203 REF		
L	0.45	0.55	0.65